## CLAIMS

What is claimed is:

1. An apparatus, comprising:

a direct memory access register adapted to hold a descriptor, said register comprising:

a command register comprising a compare enable bit and a branch enable bit;

a source address register;

a target address register; and

a descriptor address register.

2. An apparatus as in claim 1, wherein said compare enable bit is adapted to indicate a comparison operation to be performed by said direct memory access controller based on said source address register and said target address register.

3. An apparatus as in claim 1, wherein said branch enable bit is adapted to indicate a branch operation to be performed by said direct memory access controller to access another descriptor.

4. An apparatus as in claim 1, further comprising a control status register, said control status register comprising a compare status bit.

5. An apparatus as in claim 4, wherein said branch enable bit is adapted to indicate a branch operation to be performed by said direct memory access controller to access another descriptor based on said compare status bit.

6. A system, comprising:

a target;

a source;

a memory adapted to contain a first descriptor of a first type, a second descriptor of a second type, a third descriptor of a third type, and a fourth descriptor of said first type;

a direct memory access controller coupled to said memory, said direct memory access controller adapted to transfer data from said source to said target based on said first descriptor, said direct memory access controller comprising a direct memory access register to hold said first descriptor, said second descriptor, or said third descriptor, said direct memory access register comprising a command register comprising a compare enable bit and a branch enable bit.

7. A system as in claim 6, said direct memory access register further comprising a source address register and a target address register.

8. A system as in claim 7, wherein said compare enable bit is adapted to indicate a comparison operation to be performed by said direct memory access controller based on said source address register and said target address register.

9. A system as in claim 6, wherein said branch enable bit is adapted to indicate a branch operation to be performed by said direct memory access controller to fetch said fourth descriptor or said third descriptor from said memory.

10. A system as in claim 9, wherein said first descriptor is adapted to indicate data transfer by said direct memory access controller, and wherein said third descriptor is adapted to indicate no data transfer by said direct memory access controller.

11. A system as in claim 6, said direct memory access controller further comprising a control status register, said control status register comprising a compare status bit.

12. A system as in claim 11, wherein said branch enable bit is adapted to indicate a branch operation to be performed by said direct memory access controller to fetch said fourth descriptor or said third descriptor from said memory based on said compare status bit.

13. A system as in claim 11, wherein said direct memory access controller is adapted to perform a comparison operation and a branch operation based on said branch enable bit, said comparison enable bit, and said compare status bit.

14. A machine-readable medium that provides instructions, which when executed by a computing platform, cause said computing platform to perform operations comprising a method of:

fetching a first descriptor of a first type, said first descriptor identifying a first source and a first target;

transferring a first data set over a direct memory access channel from said first source to said first target based on said first descriptor;

fetching a second descriptor of a second type, said second descriptor identifying a second source, said second descriptor comprising comparison data;

fetching data from said second source identified by said second descriptor;

comparing said data fetched from said second source and said comparison data to obtain a comparison result; and

fetching one of a fourth descriptor of said first type and a third descriptor of a third type based on said comparison result.

15. A machine-readable medium as in claim 14, wherein said fourth descriptor is fetched if said comparison result indicates said data fetched from said second source fails to match said comparison data.

16. A machine-readable medium as in claim 14, wherein said third descriptor is fetched if said comparison result indicates said data fetched from said second source matches said comparison data.

17. A machine-readable medium as in claim 14, wherein said second descriptor comprises a branch enable bit and a comparison enable bit, wherein said comparing data fetched is based on said comparison enable bit in said second descriptor, and said fetching one of said fourth descriptor and said third descriptor is based on said branch enable bit in said second descriptor.

18. A machine-readable medium as in claim 14, wherein said data fetched from said second source comprises a transfer status indicator.

19. A method, comprising:

fetching a first descriptor of a first type, said first descriptor identifying a first source and a first target;

transferring a first data set over a direct memory access channel from said first source to said first target based on said first descriptor;

fetching a second descriptor of a second type, said second descriptor identifying a second source, said second descriptor comprising comparison data;

fetching data from said second source identified by said second descriptor;

comparing said data fetched from said second source and said comparison data to obtain a comparison result; and

fetching one of a fourth descriptor of said first type and a third descriptor of a third type based on said comparison result.

20. A method as in claim 19, wherein said fourth descriptor is fetched if said comparison result indicates said data fetched from said second source fails to match said comparison data.

21. A method as in claim 19, wherein said third descriptor is fetched if said comparison result indicates said data fetched from said second source matches said comparison data.

22. A method as in claim 19, wherein said second descriptor comprises a branch enable bit and a comparison enable bit, wherein said comparing data fetched is based on said comparison enable bit in said second descriptor, and said fetching one of said fourth descriptor and said third descriptor is based on said branch enable bit in said second descriptor.

23. A machine-readable medium as in claim 19, wherein said data fetched from said second source comprises a transfer status indicator.